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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/977,045	10/12/2001	Randall L. Findley	BEERS 1-2-2	3709

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EXAMINER	
FAN, CHIEH M	

ART UNIT	PAPER NUMBER
2638	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/977,045	FINDLEY ET AL.	
	Examiner	Art Unit	
	Chieh M. Fan	2638	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed 6/13/05.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 7-12 and 14-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brandt (U.S. Patent No. 5,859,550) in view of Sandusky (U.S. Patent No. 6,268,753).

Regarding claims 1, 8 and 14, Brandt teaches a synchronous sequential logic circuit, comprising: a system clock (115 in Fig. 1) that produces a reference clock signal; a plurality interconnected modules (120 in Fig. 1) that operate synchronously communicate data therebetween, each containing a phase-locked loop (PLL) (Fig. 5, col. 5, lines 15-22) that receives said reference clock signal and includes a digital feedback delay line (506 in Fig. 5). Brandt does teach that the digital feedback delay line comprises a plurality of taps, and a tap selection logic, coupled to said digital feedback delay line, for activating one of said plurality of taps and thereby insert a

corresponding delay into said PLL. Sandusky teaches a precision variable delay line whose delay is independent of process, voltage and temperature variations. The precision variable delay line comprises a plurality of taps (118, 120, 122, 124 in Fig. 4), and tap selection logic (110 in Fig. 4), coupled to said variable delay line, for activating one of said plurality of taps and thereby insert a corresponding delay (col. 5, lines 3-8). Sandusky further teaches that the total delay required by the user, as well as the delay resolution, determine the number of delay elements needed to construct the delay line, which will vary from one application to another (col. 4, lines 59-63). The amount of delay in each delay element is controlled by the delay voltage 138 (col. 5, line 11). Once the amount of delay of each delay element is set by the delay voltage for a particular application, the delay in each tap is fixed for the particular application. Also see the Fig. 3, the tap selection logic 112 selects the desired tap after the amount of delay in each delay element has been set (104, 100 in Fig. 3). That is, when the tap selection logic is making selection, each tap has fixed delay. As the feedback delay line of Brandt compensates for those delays provided by the internal clock distribution paths (col. 6, lines 30-32), it is desirable to provide precise delay compensation so as to maintain system integrity. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the precision variable delay line of Sandusky into the delay line of Brandt to precisely compensate various clock distribution delays to maintain system integrity.

Regarding claims 2, 3, 9, 10, 15 and 16, Sandusky teaches each of the taps comprises a switch (128-134 in Fig. 4). A switch is considered functionally equivalent to a 2:1 multiplexer.

Regarding claims 4, 11, and 17, Sandusky teaches that the digital feedback delay line has at least four taps (118-124 in Fig. 4).

Regarding claims 5, 12 and 18, Brandt in view of Sandusky does not specify the number of taps is 32. However, number of taps would not change the operation of the system, and the applicants do not disclose that the use of 32 taps provides an advantage or solves any stated problem. The number of taps is therefore merely a design option, dictated by system or user's requirement. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use 32 taps as required by the system.

Regard claim 19, Sandusky enables only one of the switches 128-136 (col. 4, lines 63-66, col. 5, line 4).

Regarding claims 7 and 20, Sandusky teaches that the taps selection circuit comprises a decoder (110 in Fig. 4) that receives selection signals input by the user (160 in Fig. 4) and outputs tap-selection signal to the switches (128-134 in Fig. 4). The decoder thus inherently comprises an input register (or an equivalent storage device) for receiving/processing the user's input signal and/or an output register (or an equivalent storage device) for outputting the tap-selection signal.

3. Claims 1-5, 7-12 and 14-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brandt (U.S. Patent No. 5,859,550) in view of Lee et al. (U.S. Patent No. 6,025,745, hereinafter "Lee").

Regarding claims 1, 8 and 14, Brandt teaches a synchronous sequential logic circuit, comprising: a system clock (115 in Fig. 1) that produces a reference clock signal; a plurality interconnected modules (120 in Fig. 1) that operate synchronously communicate data therebetween, each containing a phase-locked loop (PLL) (Fig. 5, col. 5, lines 15-22) that receives said reference clock signal and includes a digital feedback delay line (506 in Fig. 5). Brandt does teach that the digital feedback delay line comprises a plurality of taps, and tap selection logic, coupled to said digital feedback delay line, for activating one of said plurality of taps and thereby insert a corresponding delay into said PLL. Lee teaches a variable delay line (abstract) that is inexpensive to produce and implement (col. 2, line 40). The variable delay line (22 in Fig. 2) comprises a plurality of taps with each of said taps having a fixed delay (24 in Fig. 2, line 2 in abstract), and a tap selection logic (20 in Fig. 2), coupled to the variable delay line, for activating one of said plurality of taps and thereby insert a corresponding delay (lines 1-4 abstract). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the inexpensive variable delay line of Lee into the delay line of Brandt so as to reduce cost.

Regarding claims 2, 3, 9, 10, 15 and 16, Lee teaches each of the taps is coupled to an N:1 multiplexer (20 in Fig. 2). It is known in the art that an N:1 multiplexer is equivalent to activate one of N 2:1 multiplexers.

Regarding claims 4, 11, and 17, Lee teaches that the digital feedback delay line has at least four taps (24 in Fig. 2).

Regarding claims 5, 12 and 18, Brandt in view of Lee does not specify the number of taps is 32. However, number of taps would not change the operation of the system, and the applicants do not disclose that the use of 32 taps provides an advantage or solves any stated problem. The number of taps is therefore merely a design option, dictated by system or user's requirement. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use 32 taps as required by the system.

Regard claim 19, Lee enables only one of the taps (line 3 of abstract).

Regarding claims 7 and 20, Lee teaches that the taps selection circuit comprises a register (34 in Fig. 2).

4. Claims 1-18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brandt (U.S. Patent No. 5,859,550) in view of Furman (U.S. Patent No. 6,075,398, listed in Form 892 in the previous Office Action).

Regarding claims 1, 8 and 14, Brandt teaches a synchronous sequential logic circuit, comprising: a system clock (115 in Fig. 1) that produces a reference clock signal; a plurality interconnected modules (120 in Fig. 1) that operate synchronously communicate data therebetween, each containing a phase-locked loop (PLL) (Fig. 5, col. 5, lines 15-22) that receives said reference clock signal and includes a digital feedback delay line (506 in Fig. 5). Brandt does teach that the digital feedback delay

line comprises a plurality of taps, and a tap selection logic, coupled to said digital feedback delay line, for activating one of said plurality of taps and thereby insert a corresponding delay into said PLL. Furman teaches a variable delay line (Fig. 5) that can be tuned over a wide frequency range using standard, off the shelf, digital logic components, i.e., simple and low cost (col. 2, lines 8-10). The variable delay line comprises a plurality of taps with each of said taps having a fixed delay (510-524 in Fig. 5), and tap selection logic (108 in Fig. 1), coupled to the variable delay line, for activating one of said plurality of taps and thereby insert a corresponding delay (col. 8, lines 11-34). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the inexpensive variable delay line of Furman into the delay line of Brandt so as to reduce cost.

Regarding claims 2, 3, 9, 10, 15 and 16, Furman teaches each of the taps is coupled to a 2:1 multiplexer (510-524 in Fig. 5).

Regarding claims 4, 11, and 17, Furman teaches that the digital feedback delay line has at least four taps (24 in Fig. 2).

Regarding claims 5, 12 and 18, Brandt in view of Furman does not specify the number of taps is 32. However, number of taps would not change the operation of the system, and the applicants do not disclose that the use of 32 taps provides an advantage or solves any stated problem. The number of taps is therefore merely a design option, dictated by system or user's requirement. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use 32 taps as required by the system.

Regard claims 6 and 13, Furman teaches that the plurality of taps (510-524 in Fig. 5) are cascaded from an input to an output and said corresponding delay results from fixed delays associated with said activated one of the plurality of taps and subsequent ones of said plurality of taps between said activated one and said output (col. 7 line 61 through col. 8, line 22).

Regarding claims 7 and 20, Furman teaches that the taps selection circuit comprises a decoder (108 in Fig. 1) that receives a 3-bit control signal and output eight signals (col. 4, lines 45-46). The decoder thus inherently comprises an input register (or an equivalent storage device) for receiving/processing the 3-bit control signal and/or an output register (or an equivalent storage device) for outputting the tap-selection signal.

Response to Arguments

5. Applicant's arguments filed 6/13/05 have been fully considered but they are not persuasive.

The applicant argues that the delay elements in the delay line of Sandusky do not have fixed delay.

Response --- Sandusky teaches that the total delay required by the user, as well as the delay resolution, determine the number of delay elements needed to construct the delay line, which will vary from one application to another (col. 4, lines 59-63). The amount of delay in each delay element is controlled by the delay voltage 138 (col. 5, line

11). Once the amount of delay of each delay element is set by the delay voltage for a particular application, the delay in each tap is fixed for the particular application. Also see the Fig. 3, the tap selection logic 112 selects the desired tap after the amount of delay in each delay element has been set (104, 100 in Fig. 3). That is, when the tap selection logic is making selection, each tap has fixed delay. Further, it is well known that although a variable delay element has the advantage of flexibility, it is more difficult and more expensive to implement. Thus, even if the applicant insists that the delay amount of the delay element in Sandusky cannot be considered fixed, the replacement of a variable delay element with a fixed delay element for reducing cost is within the level of ordinary skill in the art. The usage of a fixed delay element instead of a variable delay element would not involve an inventive step.

The applicant further argues that Sandusky does not teach the delay element includes the switches but that the switches are used to select the delay element.

Response --- The applicant is reminded that the claim recites, "each of the said taps comprises a multiplexer". It is well established in the art that a "tap" in a delay line is the output of a delay element or an input to a delay element. As shown in Fig. 1A of a side reference Schieifer et al. (U.S. Patent No. 6,587,811), a tap 18 is the input/output of a delay element. On the other hand, each of the switches in Sandusky is clearly part of the delay element output. Therefore, Sandusky clearly teaches that each tap comprises a switch, which is equivalent to a 2:1 multiplexer.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chieh M. Fan whose telephone number is (571) 272-3042. The examiner can normally be reached on Monday-Friday 8:00AM-5:30PM, Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chieh M Fan
Primary Examiner
Art Unit 2638

August 20, 2005